( ) Preliminary Specifications
(V) Final Specifications

Module	**10.1”(10.1”) WUXGA 16:10 Color TFT-LCD with LED Backlight design**
Model Name	B101UAN02.1 (H/W：0A & 1A)
Note ( )	***LED Backlight without driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Trista Jiang	05/07/2012
Prepared by	**Date**
Pei-Ching Huang	05/07/2012
NBBU Marketing Division AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.0 2012/04/11	All	First Edition		
1.0 2012/05/07	All	Final Spec.		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B101UAN02.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1,920(H) x1,200(V) screen and 16.7M colors (RGB 8bits data driver) without LED backlight driving circuit. All input signals are LVDS interface compatible.

B101UAN02.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	256.42
Active Area	[mm]	216.81 X 135.50 typ
Pixels H x V		1,920x3(RGB) x 1,200
Pixel Pitch	[mm]	0.113x 0.113
Pixel Format		R.G.B. Vertical Stripe
Display Mode		AHVA, Normally Black
White Luminance (ILED=20mA) (Note: ILED is LED current)	[cd/m^2]	400 typ. (5 points average) 340 min. (5 points average)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		800 typ
Response Time	[ms]	25 typ / 35 Max
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption (Column Inversion)	[Watt]	3.65W max.[1]
Weight	[Grams]	138g max

[1] Max logic power is 1W and max backlight unit power is 2.65W. The led driver is in system.

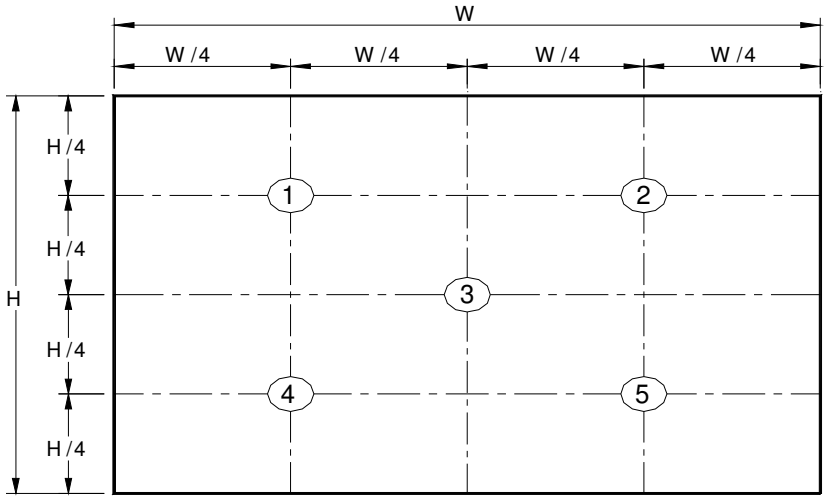
Physical Size	[mm]		Min.	Typ.	Max.
		Length	228.95	229.45	229.95
		Width	148.70	149.20	149.70
		Thickness	-	-	2.50 (Panel Side) 5.00 (PCBA Side)
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.25			
Surface Treatment		Glare, Hardness 3H,			
Support Color		16.7M colors (RGB 8-bits)			
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -20 to +60 -30 to +70			
RoHS Compliance		RoHS Compliance			

2.3 Optical Characteristics

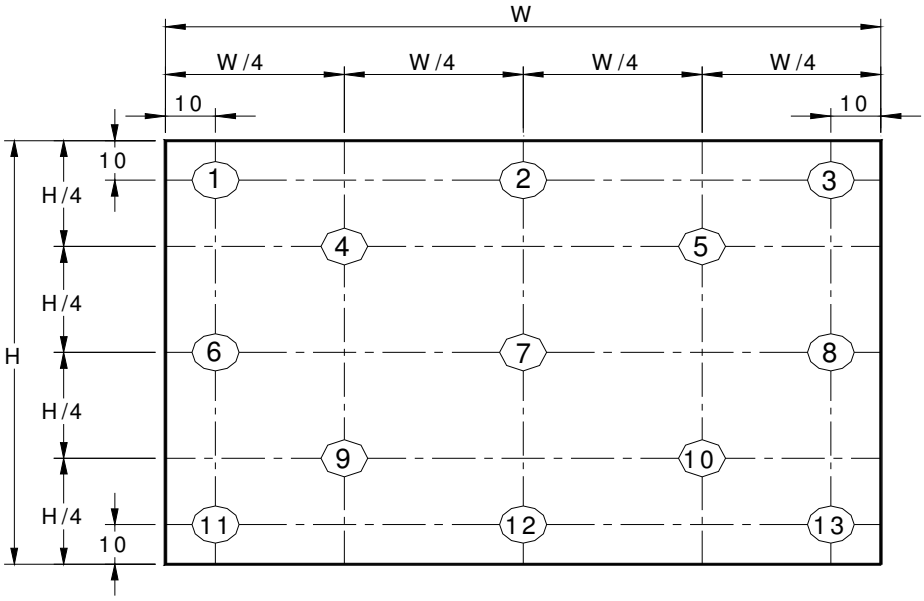
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R	Horizontal (Right) CR = 10	80	89	-	degree	4, 9
		θ_L	(Left)	80	89	-		
		ψ_H	Vertical (Upper) CR = 10	80	89	-		
		ψ_L	(Lower)	80	89	-		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.5		2, 3, 4
Contrast Ratio		CR		-	800	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	13	18	msec	4, 8
		T_f	Falling	-	12	17		
		T_{RT}	Rising + Falling	-	25	35		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.589	0.619	0.649		4
		Ry		0.304	0.334	0.364		
	Green	Gx		0.276	0.306	0.336		
		Gy		0.575	0.605	0.633		
	Blue	Bx		0.118	0.148	0.178		
		By		0.030	0.060	0.090		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	68	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

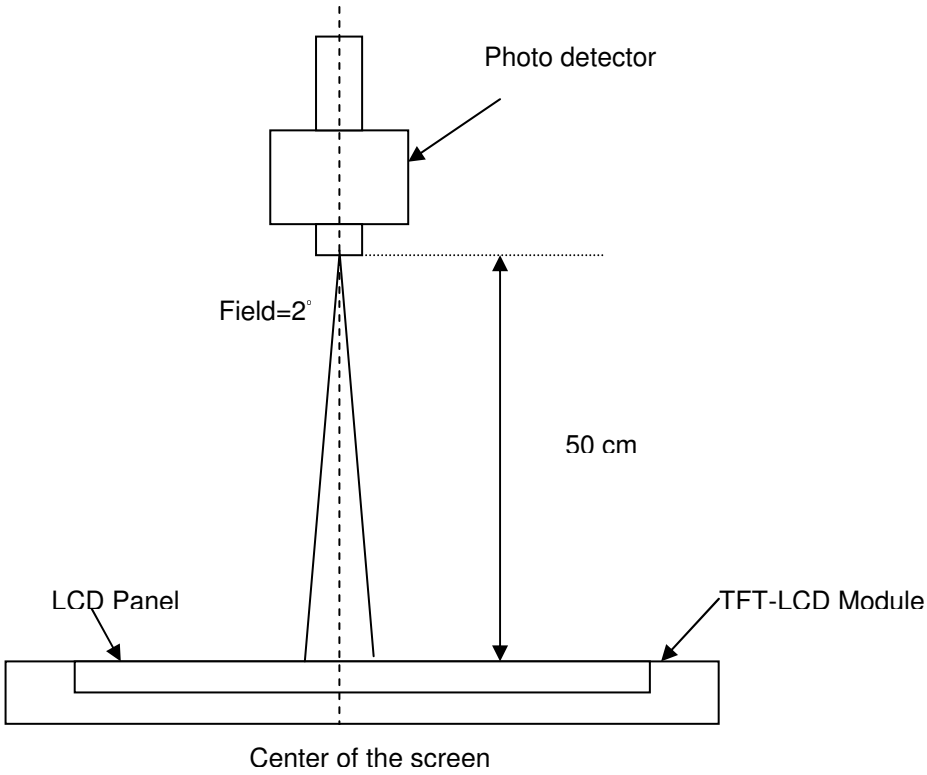
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

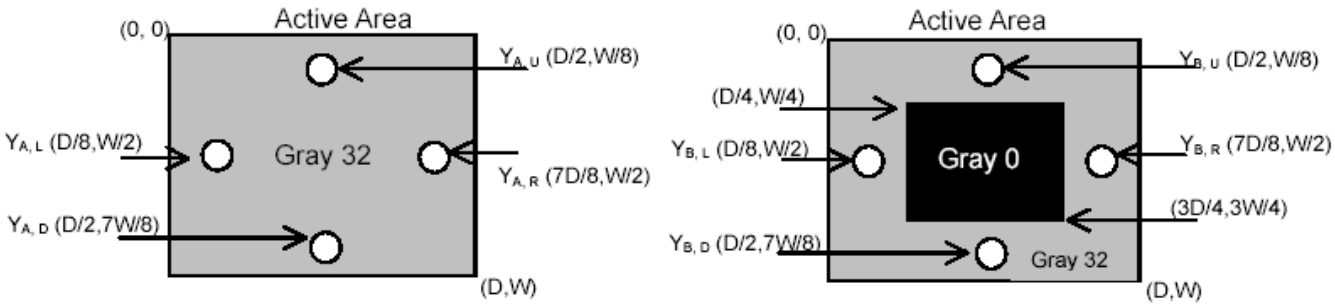
Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

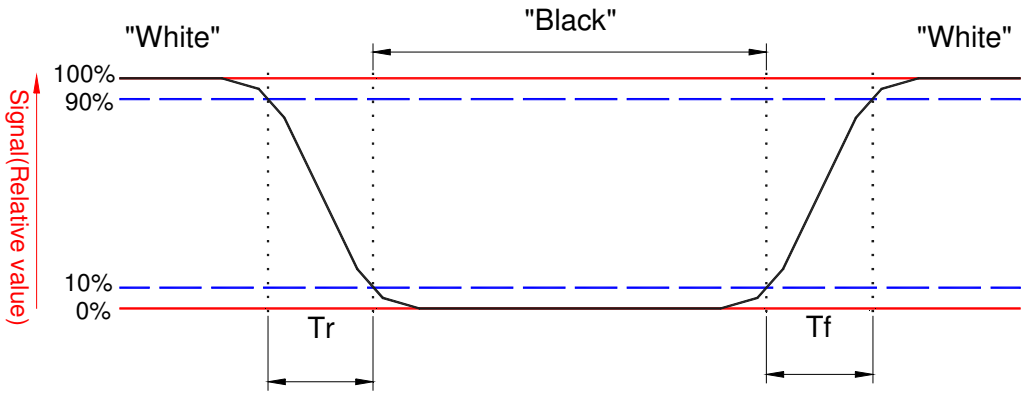
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



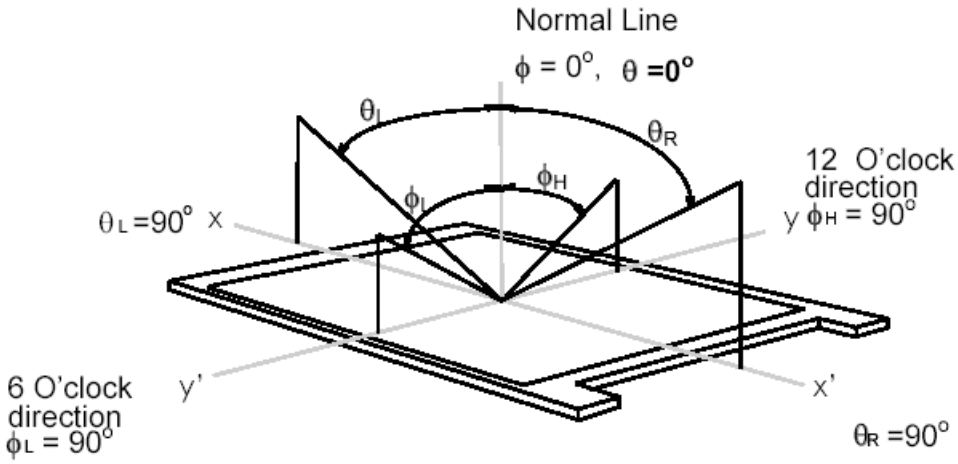
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



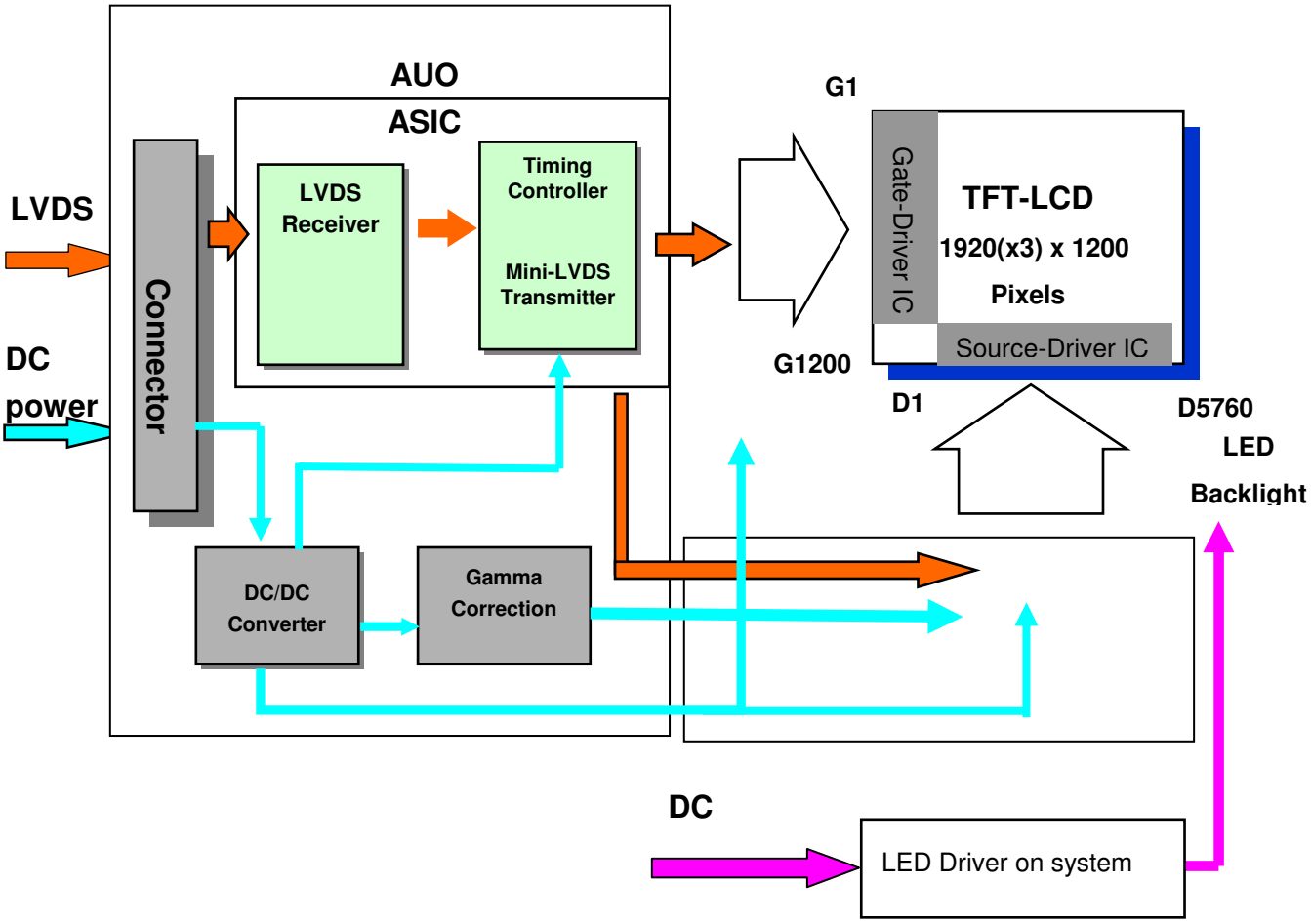
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 50 Pin two channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Touch Sensor

Item	Symbol	Min	Max	Unit	Conditions
Touch Sensor Power Voltage	Vin	4.5	5.5	[Volt]	

4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	-20	+60	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-30	+70	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

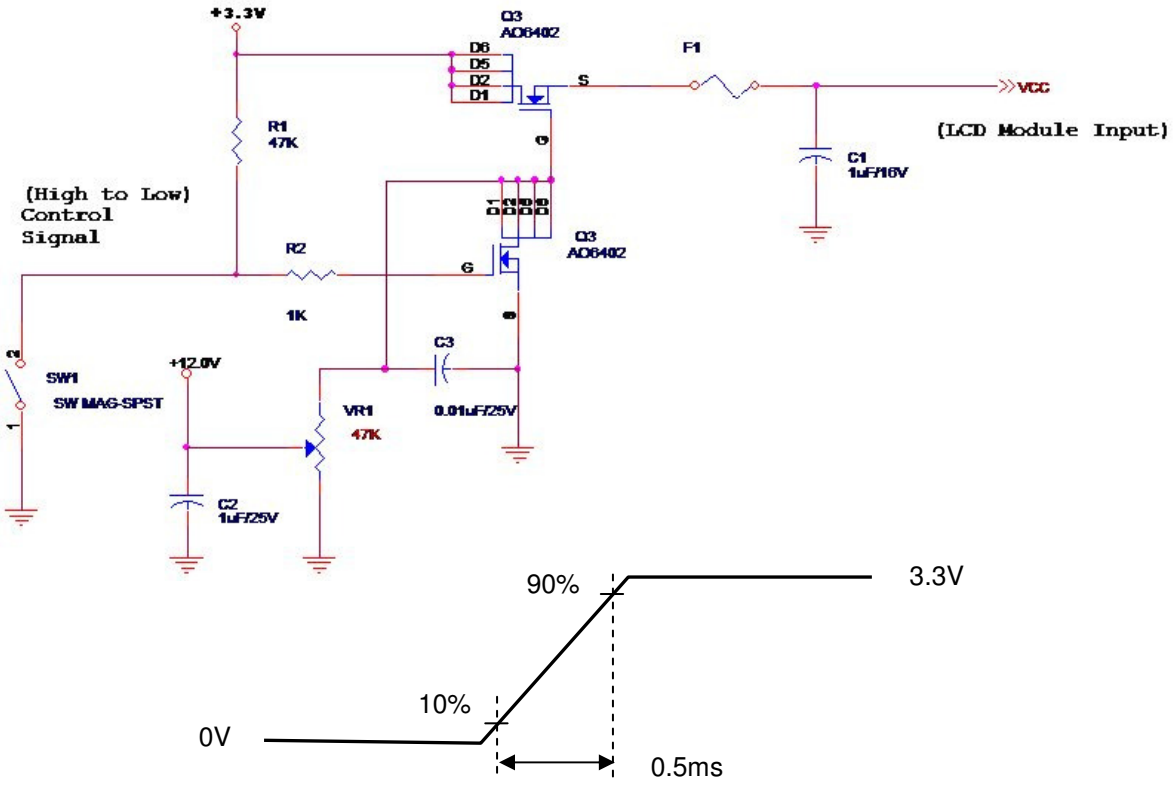
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.09	[Watt]	Note 1
IDD	IDD Current	-	272	303	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2 : Measure Condition



Vin rising time

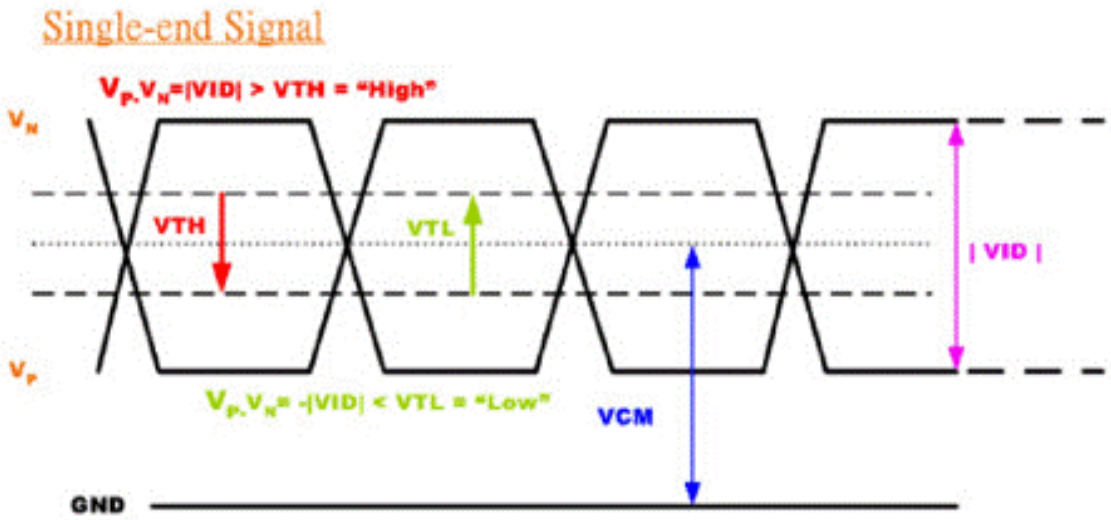
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)	-	100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	Note 1	[Watt]	(Ta=25℃), Note 1
LED Life-Time	N/A	10K		-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency and depends on system LED driver design.

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

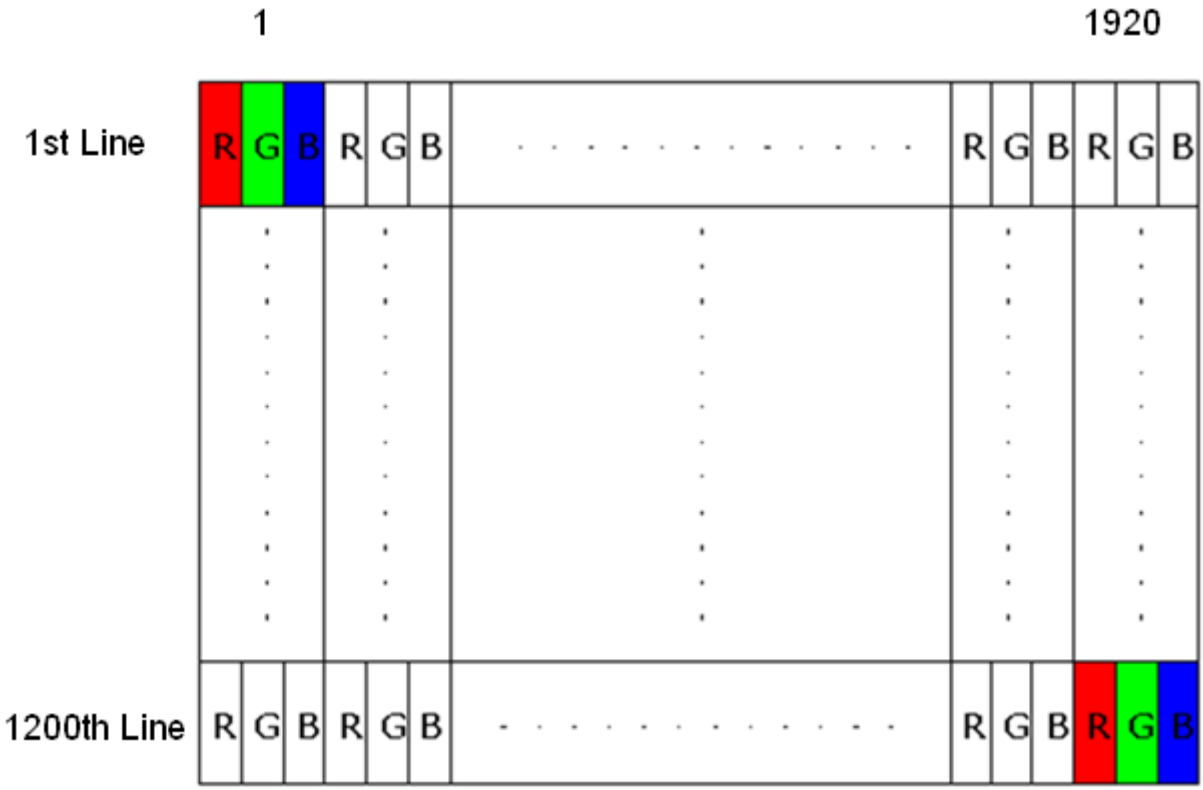
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED (Note 1)	21.6	24.0	26.4	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	130		16K	Hz	
PWM Duty Ratio	Duty	5		100	%	

Note1: LED Power Supply is evaluated by Nichia LED.

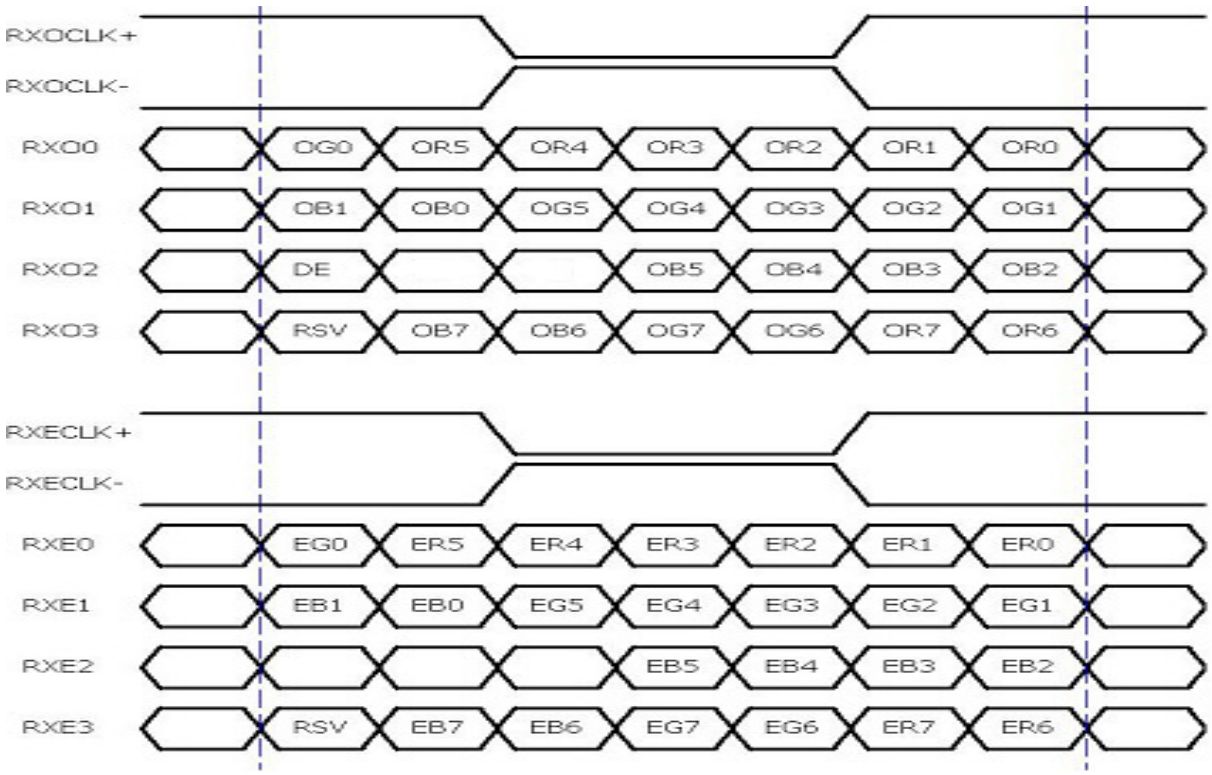
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7(MSB) Green Data 6 Green Data 5 Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2	Blue Data 8(MSB) Blue Data 7 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.

B1 B0	Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note1: DE Mode Only.
Note 2: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I_PEX or Compatible
Type / Part Number	I_PEX 20455-050E-12 or compatible
Mating Housing/Part Number	I_PEX 20453-050T-11 or compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No connection
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VDDEDID	EDID +3.3V Power
5	NC	No connection
6	CLK_EDID	EDID Clock Input
7	DATA_EDID	EDID Data Input
8	GND	Ground
9	RXOIN0N	Negative LVDS Differential Data INPUT for odd pixel
10	RXOIN0P	Positive LVDS Differential Data INPUT for odd pixel
11	GND	Ground
12	RXOIN1N	Negative LVDS Differential Data INPUT for odd pixel
13	RXOIN1P	Positive LVDS Differential Data INPUT for odd pixel
14	GND	Ground
15	RXOIN2N	Negative LVDS Differential Data INPUT for odd pixel
16	RXOIN2P	Positive LVDS Differential Data INPUT for odd pixel
17	GND	Ground
18	RXOCLKINN	Negative LVDS Differential Clock INPUT for odd pixel
19	RXOCLKINP	Positive LVDS Differential Clock INPUT for odd pixel
20	GND	Ground
21	RXOIN3N	Negative LVDS Differential Data INPUT for odd pixel

22	RXOIN3P	Positive LVDS Differential Data INPUT for odd pixel
23	GND	Ground
24	RXEIN0N	Negative LVDS Differential Data INPUT for even pixel
25	RXEIN0P	Positive LVDS Differential Data INPUT for even pixel
26	GND	Ground
27	RXEIN1N	Negative LVDS Differential Data INPUT for even pixel
28	RXEIN1P	Positive LVDS Differential Data INPUT for even pixel
29	GND	Ground
30	RXEIN2N	Negative LVDS Differential Data INPUT for even pixel
31	RXEIN2P	Positive LVDS Differential Data INPUT for even pixel
32	GND	Ground
33	RXECLKINN	Negative LVDS Differential Clock INPUT for even pixel
34	RXECLKINP	Positive LVDS Differential Clock INPUT for even pixel
35	GND	Ground
36	RXEIN3N	Negative LVDS Differential Data INPUT for even pixel
37	RXEIN3P	Positive LVDS Differential Data INPUT for even pixel
38	GND	Ground
39	DCR_EN (CABC_EN)	Dynamic backlight control
40	PWM_IN	System PWM signal input for dimming
41	PWM_OUT	Panel PWM signal output to system
42	NC	NC
43	LED_CA5	LED Cathode 5
44	LED_CA4	LED Cathode 4
45	LED_CA3	LED Cathode 3
46	LED_CA2	LED Cathode 2
47	LED_CA1	LED Cathode 1
48	NC	No connection
49	VLED Output	LED Backlight power
50	VLED Output	LED Backlight power

6.5 Interface Timing

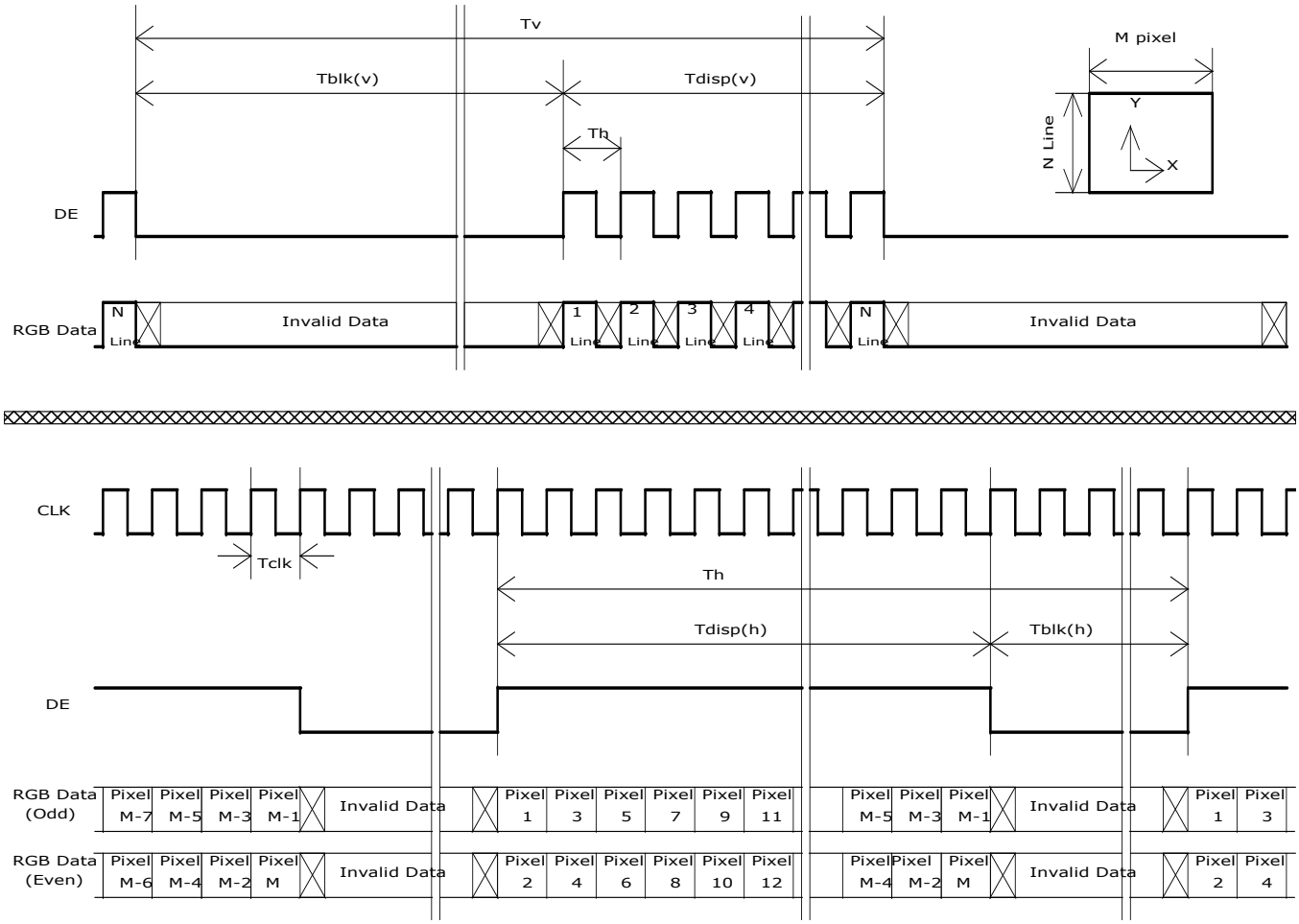
6.5.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	--	60	---	Hz
Clock frequency		1/ T_{Clock}	64	76.36	85	MHz
Vertical Section	Period	T_V	1210	1212	1240	T_{Line}
	Active	T_{VD}	1200			
	Blanking	T_{VB}	10	12	40	
Horizontal Section	Period	T_H	1034	1050	1140	T_{Clock} (Note 2)
	Active	T_{HD}	960			
	Blanking	T_{HB}	74	90	180	

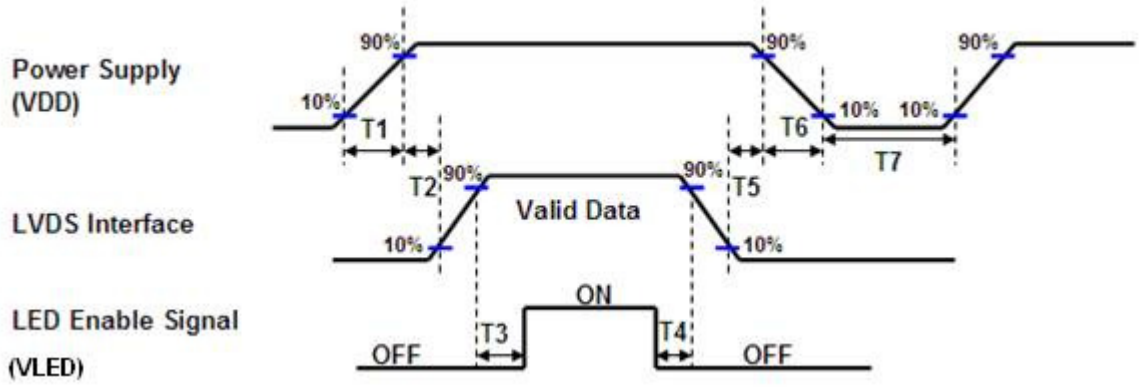
Note1 : DE mode only
Note 2: Dual LVDS Channel

6.5.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing

Parameter	Value Min.	Value Max.	Units
T1	0.5	10	ms
T2	0	50	ms
T3	200	-	ms
T4	200	-	ms
T5	0	50	ms
T6	0	10	ms
T7	500	-	ms

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 240h	
High Temperature Operation	Ta= 60℃, Dry, 240h	
Low Temperature Operation	Ta=-20℃, 240h	
High Temperature Storage	Ta= 70℃, 240h	
Low Temperature Storage	Ta= -20℃, 240h	
Thermal Shock Test	Ta=-30℃(30min) ~70℃(30min), 20cycles condition.	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

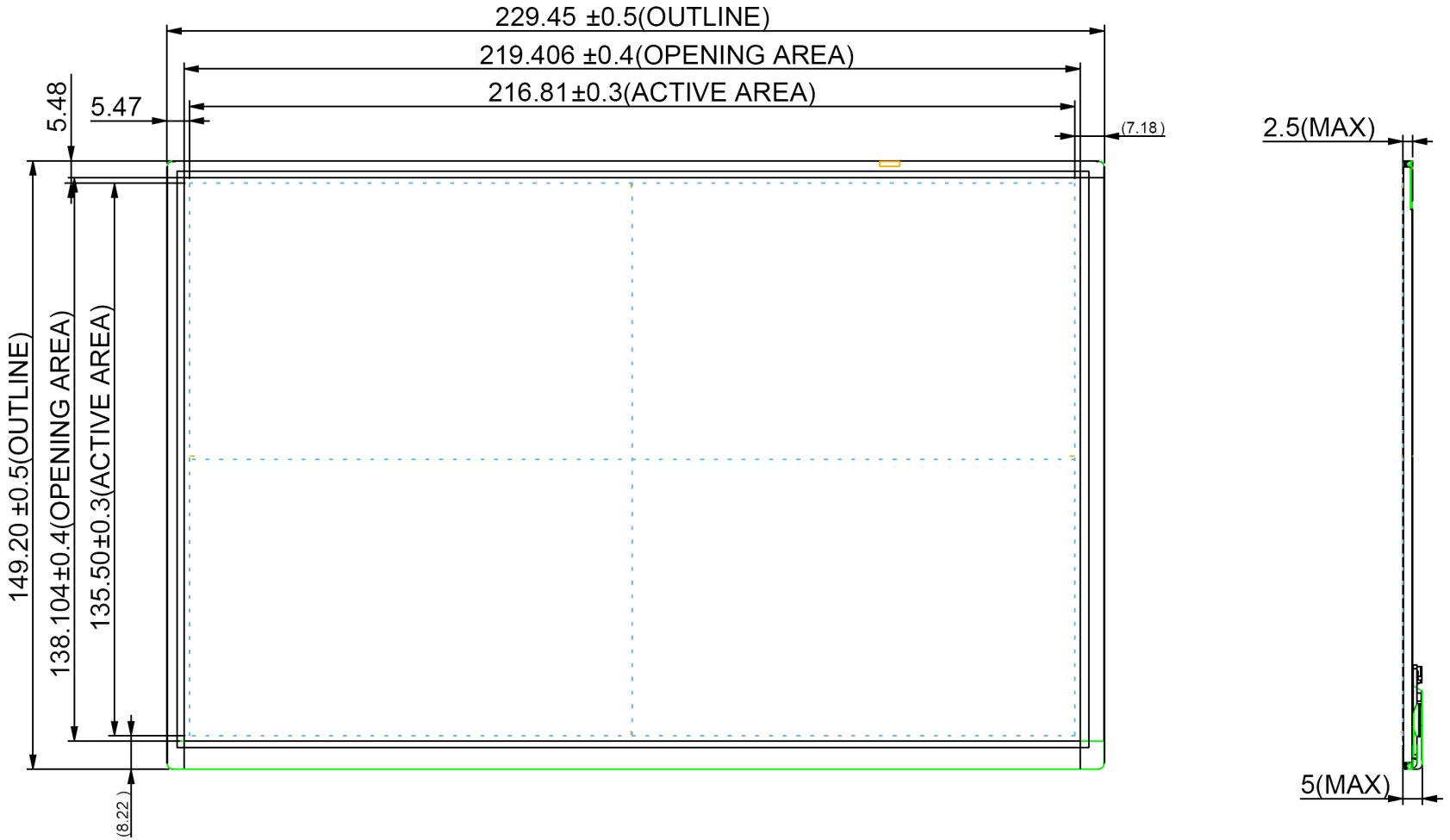
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

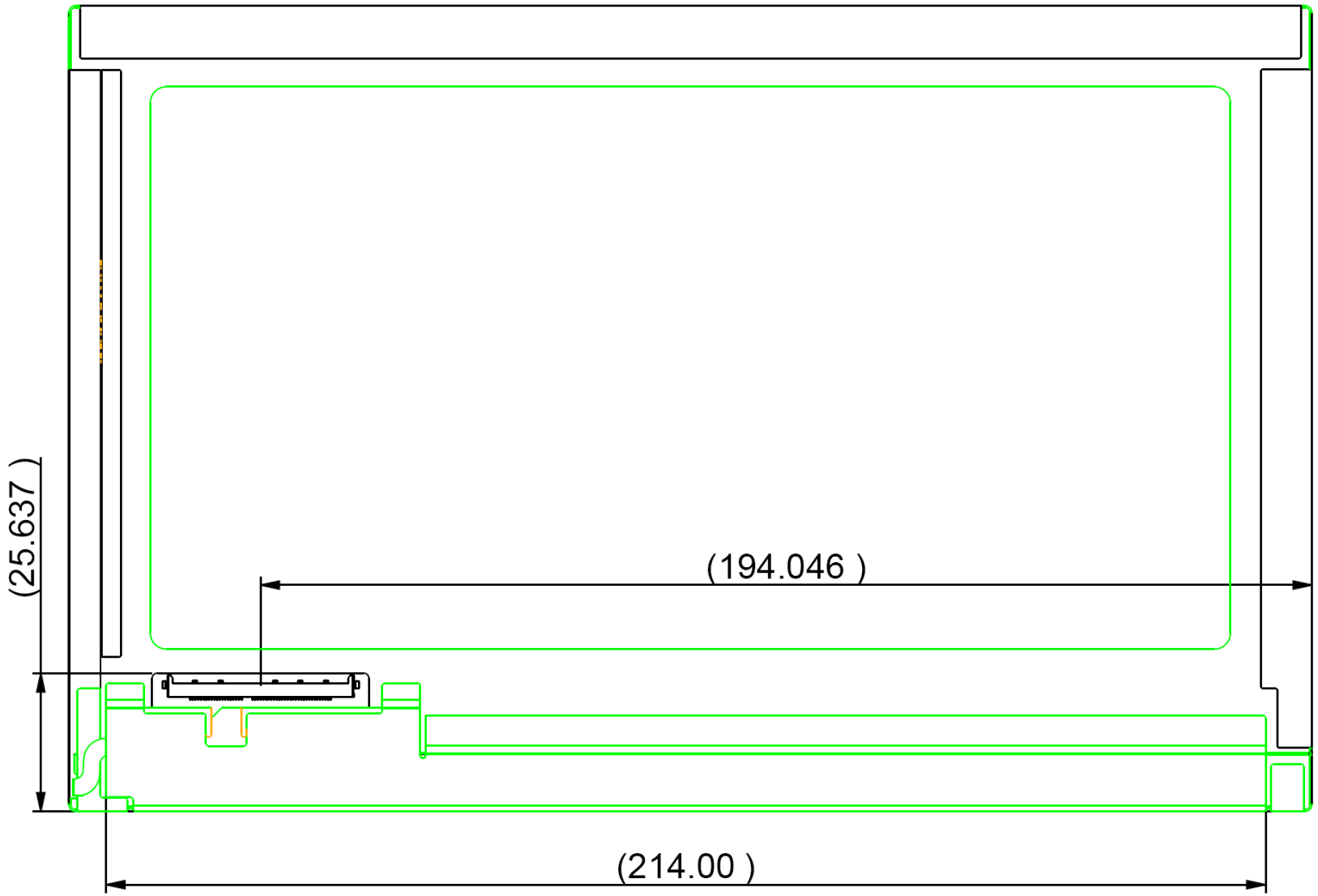
8.1 LCM Outline Dimension

8.1.1 Front View



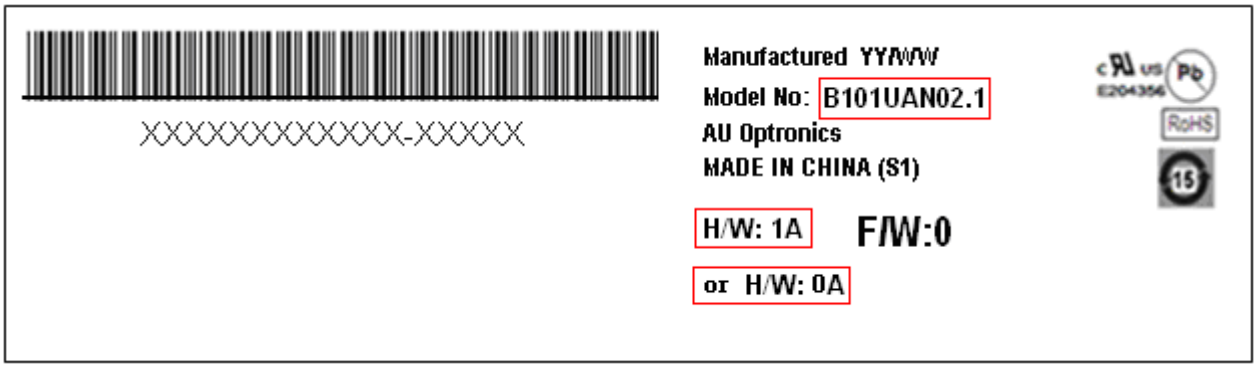
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

8.1.2 Rear View

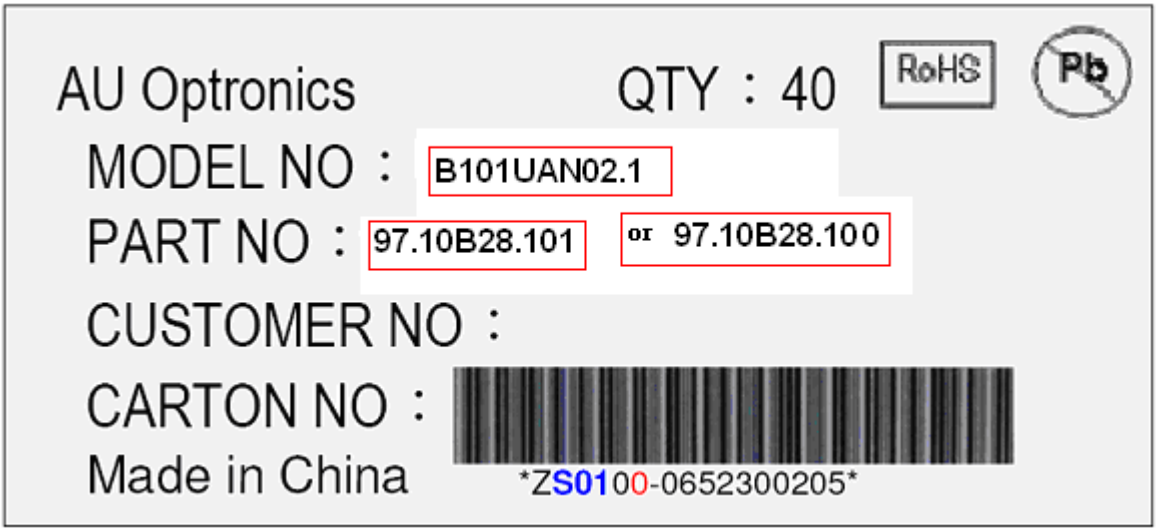


9. Shipping and Package

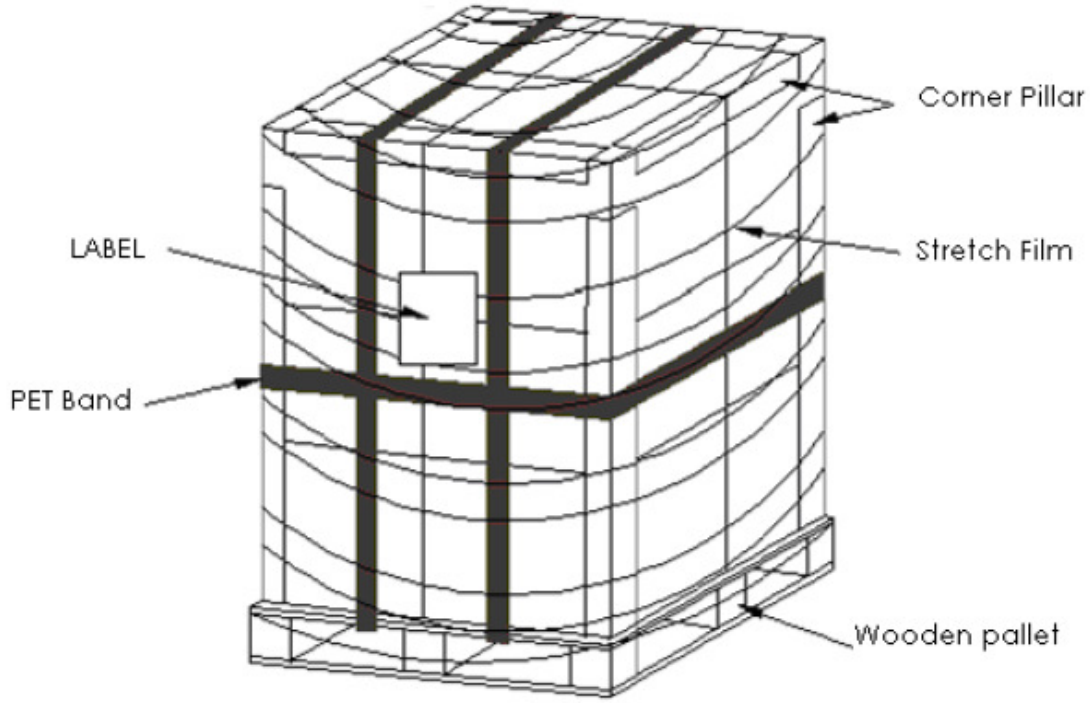
9.1 Shipping Label Format



9.2 Carton Label Format



9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

H/W: 0A

HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	D8	11011000	216	
0B	hex, LSB first	22	00100010	34	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	15	00010101	21	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	A0	10100000	160	
15	**Max H image size** *(rounded to cm)*	16	00010110	22	
16	**Max V image size** *(rounded to cm)*	0E	00001110	14	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	66	01100110	102	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5	11110101	245	
1B	Red x **(Upper 8 bits)**	A2	10100010	162	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	4F	01001111	79	
1E	Green y	9A	10011010	154	
1F	Blue x	24	00100100	36	
20	Blue y	10	00010000	16	
21	White x	4F	01001111	79	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	

2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	90	10010000	144	
37	Pixel Clock/10000 USB	3D	00111101	61	
38	Horz active **Lower 8bits**	80	10000000	128	
39	Horz blanking **Lower 8bits**	B4	10110100	180	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	70	01110000	112	
3B	Vertical Active **Lower 8bits**	B0	10110000	176	
3C	Vertical Blanking **Lower 8bits**	32	00110010	50	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	40	01000000	64	
3E	HorzSync. Offset	3C	00111100	60	
3F	HorzSync.Width	3C	00111100	60	
40	VertSync.Offset : VertSync.Width	AA	10101010	170	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	D8	11011000	216	
43	Vertical Image Size **Lower 8bits**	88	10001000	136	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	

5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	30	00110000	48	0
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	55	01010101	85	U
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	54	01010100	84	T
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	32	00110010	50	2
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	32	00110010	50	2
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	CC	11001100	204	

H/W: 1A

Address	FUNCTION	Value	Value	Value	Note
HEX		**HEX**	**BIN**	**DEC**	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	

0A	Product Code	D8	11011000	216	
0B	hex, LSB first	22	00100010	34	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
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1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	F5	11110101	245	
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2A	Standard timing #3	01	00000001	1	
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36	Pixel Clock/10000 LSB	90	10010000	144	
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3C	Vertical Blanking **Lower 8bits**	32	00110010	50	
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43	Vertical Image Size **Lower 8bits**	88	10001000	136	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0	
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46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	

6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	30	00110000	48	0
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	55	01010101	85	U
76	Manufacture P/N	41	01000001	65	A
77	Manufacture P/N	54	01010100	84	T
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	32	00110010	50	2
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	32	00110010	50	2
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	CB	11001011	203	